Fully Vacuum Deposited Perovskite Solar Cells in Substrate Configuration

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Summary:

A solar cell in the substrate configuration has an opaque back metal electrode on the substrate and a transparent conducting oxide (TCO) electrode at the front of the active stack. This allows the area of the solar cell to be scaled with relative ease as the incorporation of metal gridlines on the top TCO electrode, which is necessary to counter the resistive losses of the latter, do not influence the processing of the underlying device layers. Here, we demonstrate the fabrication of perovskite solar cells in the substrate configuration using vacuum deposition methods. The best cells have a power conversion efficiency (PCE) of ~19%, which is comparable to that of the simultaneously fabricated conventional superstrate cells (PCE ~19.5%). Moreover, both the substrate and superstrate devices exhibit similar thermal stability at 85 °C in N_2 environment, maintaining > 80% of their original PCE for more than 550 hours.

Keywords:

Substrate configuration, Perovskite solar cell, Thermal evaporation, Pulsed Laser deposition

Introduction:

Perovskite solar cells (PSCs) have rapidly advanced, attaining power conversion efficiencies (PCEs) above 25% for single-junction cells,[1] as well as significantly improved device stability. The above high values of PCE, however, are demonstrated on lab-scale, small-area (~0.1 cm^2) PSCs fabricated on transparent conductive oxide (TCO) coated glass substrates in the superstrate configuration.[2] Due to the small areas of these cells, the resistive losses due to the inadequate conductivity of the TCO electrodes are negligible and their PCE values are not compromised. Superstrate devices, that employ a TCO as the back- or bottom-contact (bottom-TCO) cannot be scaled up straightforwardly as the resistive losses of the TCO would become significant, limiting the current flow and the fill factor (FF) of the cell.[3] Metal grids could be incorporated on the bottom-TCO to counter these losses,[3] however, that complicates the subsequent processing of the device[4,5]. The metal grids would need to have a minimum cross-sectional area to conduct a required magnitude of current, implying that their height should be at least one micron to keep their width limited.[5] Such a high thickness of the metal gridlines, however, will affect the deposition and uniformity of the subsequently deposited layers including the perovskite film, and thus the performance of the resultant cell (see **Figure S1**).[4,5]

Alternatively, PSCs could also be fabricated in the substrate configuration. In this case, contrary to superstrate configuration, a transparent front electrode is positioned on top of the active stack. This allows the area of the devices to be scaled with relative ease as the metal gridlines can be placed on the top-electrode, typically a TCO, without influencing the prior processing of the underlying device layers.[4] Despite this advantage, the number of reports on PSCs in substrate configuration remains scarce.[6,7,16,17,8–15] This could be partly due to the additional challenges associated with the processing of PSCs on metal thin films or foils than on bottom-TCOs or in superstrate configuration, and the deposition of the top-TCO electrodes without damaging the underlying device layers.[18]

To date, most PSCs in substrate configuration were prepared in the n-i-p configuration, in particular on titanium foils as these foils have an intrinsically formed TiO_2 layer on their surface which is a known electron transporting layer.[7,8,10,12] The highest PCEs obtained for p-i-n and n-i-p PSCs in substrate configuration are 16.4% and 15.9%, respectively.[6,17] Given the advantages of fabricating large area devices in the substrate configuration and the large gap between the highest

PCE values of PSCs in superstrate and substrate configuration, it is important to advance the development of PSCs in the substrate architecture.

In this work, we demonstrate the complete fabrication of p-i-n perovskite solar cells in substrate configuration using scalable vacuum deposition processes. The solar cells employ a co-evaporated formamidinium methylammonium lead iodide (FAMAPI) perovskite layer and demonstrate a maximum power conversion efficiency (PCE) of ~19%, which is comparable to that of the simultaneously fabricated superstrate cells (PCE ~19.5%). The devices in the substrate configuration show on average a higher short-circuit current density than the superstrate devices which is attributed to the lower reflectance losses in the former. Next, we observe that the encapsulated devices of both the configurations have a similar thermal stability at 85 °C in N_2 environment, maintaining > 80% of their original PCE for more than 550 hours. Our findings may contribute towards the development of large-area, efficient, and thermally stable fully vacuum-deposited PSCs.

Results and Discussion:

The device stacks employed for fabricating PSCs in the superstrate and substrate configurations (here by denoted as superstrate devices and substrate devices, respectively) are shown in **Figure 1a.** We incorporated a formamidinium methylammonium lead iodide (FAMAPI) perovskite composition grown by a three source co-sublimation process in the PSCs due to its relatively high thermal stability, and absorbance range.[19,20] For the substrate devices, we used a ~45 nm thermally evaporated aluminum thin film with a sheet resistance of 1.5 **Ω**/sq. as the reflective, back-metal electrode. It was deposited on a seed layer of 1nm silver /5 nm MoO_x to obtain a smooth and robust film and to ensure good adhesion to the glass substrate. The atomic force microscope images, as well as the derived roughness values, and the reflectance spectra of the aluminum films grown with and without the seed layer are shown in **Figure S2**. On top of the aluminum electrode, we deposited a ~45 nm layer of Indium Tin Oxide (ITO) using a pulsed laser deposition (PLD) method at a low pressure of 0.007 mbar.[21] This ITO layer was deposited to ensure a similar interface for the hole transport layer (HTL) in both device configurations. As HTL we employed 3 nm layer of 2,2',7,7'-tetra(N,N-di-*p*-tolyl)amino-9,9-spirobifluorene (Spiro-TTB).[22,23] This material was used as it can form ohmic-like contact for holes with ITO without the aid of any high work function layer at their interface. Additionally, it has been used to prepare thermally stable p-

i-n PSCs in the superstrate configuration.[24] Subsequently, the FAMAPI perovskite layer was grown by co-evaporating PbI_2 and MAI, and FAI (see experimental section for the details). After the perovskite deposition, the samples were annealed at 100 °C for 10 minutes, and then the electron transporting layers (ETL), consisting of 20 nm fullerene C_{60} and 8 nm BCP were deposited. All the layers starting from the HTL to bathocuproine (BCP) were simultaneously evaporated on both the superstrate and substrate samples to ensure the same device processing conditions. We did this to enable a fair comparison between the performances of the resultant superstrate and substrate devices. For the substrate configuration the top-ITO electrode (~75 nm, sheet resistance of 50 Ω/sq) was deposited on the ETL using the PLD method due to its efficacy in depositing TCO layers directly on top of the soft organic layers without damaging them.[21,25,26] The top-electrode consisted of a thin (~8 nm) buffer layer of ITO deposited at a relatively high pressure of 0.042 mbar and a primary, thick (~67 nm), dense, and conductive ITO layer deposited subsequently at a low pressure of 0.007 mbar similar to the hole extracting contact (see methods for more details). The 'soft' deposited buffer layer was used to protect the underlying device layers from the 'harsh' deposition of the primary, conductive ITO layer. Without such a layer the devices are shunted due to direct contacts between the top and bottom ITO layers as can be seen from the J-V curves of the devices obtained in the dark (**Figure S3**). Next, silver fingers were deposited on top of the ITO electrode in the substrate devices to facilitate charge extraction without incurring resistive losses. Al_2O_3 was used as an encapsulation layer and deposited after the Ag fingers using atomic layer deposition (ALD) as this ensures a pinhole free layer. The ITO thickness of the top electrode in the case of substrate configuration is only ~75 nm as it allows for low reflectance losses in the device. Although it exhibits a higher sheet resistance of ~50 Ω/sq, the deposition of metal fingers around ITO electrodes prevents the occurrence of resistance losses during the charge extraction process from the device (See optical image of the device with the shape of Ag fingers around the top-ITO electrodes **Figure S5**).

In the superstrate device 100 nm of Ag was deposited on the ETL as the opaque top electrode. Both device stacks were finalized by depositing a 90 nm LiF antireflection layer on the light-incidence side. For the superstrate device the LiF was evaporated on the glass substrate, while in the case of the substrate configuration the LiF was deposited on top of the alumina encapsulation

layer. Note that while both the substrate and superstrate PSCs are fabricated in p-i-n configuration, the light is incident on them from opposing sides of the stack, i.e., n-side and p-side, respectively.

The cross-sectional, scanning electron microscope (SEM) image of the substrate device reveals a perovskite film thickness of 570 ± 10 nm, as well as uniformly and conformally deposited layers on top of the perovskite film (**Figure 1b**). This demonstrates the efficacy of sublimation and PLD processes in depositing planar and conformal layers, a requisite for fabricating substrate devices. The cross-sectional SEM image also reveals the presence of large grains in the FAMAPI layer (**Figure 1b**, see a larger cross-sectional SEM image in **Figure S4**). The absorbance and photoluminescence spectra of the annealed perovskite films are shown in **Figure 2a**. The photoluminescence peak position indicates that the FAMAPI perovskite has an approximate band gap of 1.54 eV. We measured the X-ray diffraction (XRD) pattern of the FAMAPI layers in the two device configurations to verify any differences in the texture of the perovskite due to the differences in their underlying layers and the results are shown in **Figure 2b**. The diffractograms were obtained from the measurement of fully finished superstrate and substrate devices. The FAMAPI films in both the cases exist in the cubic α-phase as revealed by the whole pattern Le-Bail fit of the diffractograms (**Figure S6 and Table S1**). There is no preferred orientation with respect to the substrate as reflected by the presence of intense diffraction peaks along the [100] and [210] directions. The comparable intensities of [100] and [210] diffraction peaks indicate an approximate x value of 0.4-0.5 in the above $FA_{1-x}MA_xPbI_3$ layers based on our previous analysis.[27] In addition to the diffraction peaks of the cubic perovskite phase, the diffractograms also reveal the presence of PbI_2 and the absence of the yellow non-perovskite phase (space group *P63/mcm*) in the perovskite film. Small differences in the relative intensities of some diffraction peaks when comparing the superstrate and substrate devices can be observed. The PbI_2 peak at 2Θ ~ 12.6° and the ratio of intensities of the (100) perovskite peak at 2Θ ~ 14° with (110) and (210) perovskite peaks at 2Θ ~19.8° and 31.6°, respectively, (i.e., $Intensity_{(100)}/Intensity_{(110)}$ and $Intensity_{(100)}/Intensity_{(210)}$) are different for the perovskite layers in the two device configurations (**Table S2**). This may indicate a slightly different growth of the FAMAPI layer in the two cases. The main difference between the two device configurations is the presence of a crystalline ITO layer in the superstrate device. This, in particular due to orientation of its crystallites along the non-axial (222) plane may provoke a slightly different perovskite growth. This is in agreement with a previous observation we made for a methylammonium lead iodide perovskite film grown

on a crystalline bottom-ITO-based substrate, which also had a lower intensity of the (100) diffraction peak than for the same perovskite deposited on an ITO free substrate.[28]

The external quantum efficiency (EQE) spectra show the differences in the current generation in the two device configurations (**Figure 3a)**. To analyze the origin of the above differences, as well as, to qualitatively compare the extent of parasitic absorption losses in the two types of devices, we simulated their '1-R' (R is the device reflectance) spectrum using a home-built transfer matrix program (see methods), and compared them with their respective EQE spectrum (**Figure 3b**). For wavelengths (λ) greater than 400 nm, assuming negligible transmittance of light, the 1-R spectrum of a device should be similar to the total absorption spectrum of the device. We observed that the features of the 1-R spectra of the devices resemble their respective EQE spectra. The 1-R spectra of the two types of devices indicate that the cavity-dominant region starts at λ ~600 nm, as reflected by the onset of a 'peak' (local maxima) and a 'valley' (local minima) in the case of superstrate and substrate configurations, respectively. For λ below ~495 nm, the lower EQE of the substrate device is ascribed to the high parasitic absorption of light by the front C_{60} layer in the former, as well as its higher reflection of light for λ up to ~ 470 nm. For λ between ~495 nm and ~625 nm, the substrate device exhibits a higher EQE than its superstrate counterpart due to lower reflection of light and despite the continued (though relatively lower than before) parasitic absorption of light by the C_{60} layer. Lowering the C_{60} layer thickness to its minimum required value or replacing it with a more visible-transparent electron transport layer is expected to increase the above range of enhanced absorption of light, and consequently, the short circuit current density (J_{sc}) of the resultant substrate device. In the case of the superstrate device, on the other hand, we note that there is only a small difference in the magnitude of simulated 1-R and EQE values in the beer-lambert absorption region of the perovskite, reflecting the presence of minimal parasitic absorption losses in the device in the above spectrum. This is in agreement with the transmittance spectra for the semi-transparent electrode and adjacent layers for the two types of device configurations as shown in **Figure S7**.

In the cavity-dominant region, the EQE spectrum of a device is influenced by the interference of light. Upon close inspection of the EQE spectra in the above region, we observe that the positions of local maxima and minima in the EQE spectrum of the two kinds of devices do not match with

each other indicating the possibility of difference in the perovskite layer thickness in the two device configurations. We carried out optical simulations to probe this and the results confirm that indeed the shape of simulated 1-R spectrum of the substrate and superstrate devices only match well with that of their respective EQE spectrum when we assume different perovskite thicknesses of 560 nm and 500 nm, respectively. The thickness of 560 nm for the perovskite layer in the substrate type device is in reasonable agreement with the measured thickness of ~ 570 nm (from the cross-sectional SEM image of the substrate device (Figure 1c). The simulated 1-R spectra of the substrate and superstrate devices shown in **Figure 3b** are obtained assuming a perovskite thickness of 560 nm and 500 nm, respectively. For experimental comparison of the perovskite film thicknesses, we re-fabricated the FAMAPI layers again on a thin layer of Spiro-TTB on the substrates with and without the crystalline-bottom ITO (**Figure S8**). The FAMAPI layer was observed to be approximately 10 % thicker on the substrate without the crystalline ITO layer (similar to substrate device) thus corroborating the prediction of the above optical simulations. It further indicates that the presence or absence of a crystalline-bottom ITO layer is responsible for the observed difference in the perovskite thicknesses in the two device configurations. This is the first report that demonstrates a difference in the final perovskite film thicknesses in the same deposition due to difference(s) in their underlying layers.

The current density (J)-Voltage (V) curves and the corresponding values of the PCE parameters (in reverse scan) of the best device of the two configurations under simulated 1 sun illumination are shown in **Figure 3c**. The highest efficiencies obtained for the superstrate and substrate devices, obtained in the reverse scan are 19.45% and 19.01% respectively. To the best of our knowledge, the latter value is the highest reported for the PSCs fabricated in substrate configuration (**Figure S9**). The statistical comparison of the performance of the devices (**Figure 3d** and **Table S3**) reveals a higher average value of the PCE for the superstrate devices than their substrate counterpart. This is caused by their slightly higher average open circuit voltage (V_{oc}), and fill factor (FF) values. The substrate devices on the other hand have a higher average J_{sc} value due to their lower reflectance losses as suggested by the simulated 1-R and EQE spectra, and despite the parasitic absorption of light from the front C_{60} layer. The dark J-V curves of the devices indicate that the slightly lower FF value of the substrate devices maybe caused by a higher series resistance and a lower shunt resistance (**Figure S10a**). The sequence of layers from the Spiro-TTB layer to that of the BCP layer in two device configurations was deposited at the same time. Hence, it is

most likely that the higher series resistance in the substrate device originates from either the bottom Al/ITO hole extracting contact and/or the top BCP/ITO electron extracting contact. To check if this originates from the electron extracting contact, we fabricated two kinds of devices with the following top contacts: BCP/ITO plus Ag fingers and BCP/Ag. The dark J-V curves of the resultant devices, however, showed negligible difference in their series resistance (**Figure S10b**), implicitly indicating the origin of the higher series resistance in the substrate device to be at its hole extracting contact.

Next, both the substrate and superstrate devices were stressed at 85 °C on a hot plate and in N_2 atmosphere/ambient to evaluate their thermal stability. The two types of devices demonstrated comparable thermal stability, retaining 80% of their average initial efficiency for more than 550 hours, as well as similar degradation pattern of the PCE parameters (**Figure 4**). This reflects that the fabricated substrate devices virtually possess the same robustness against thermal stress as their superstrate counterparts. All parameters reduce over time although the FF shows some recovery after 400 hours of stressing. We measured the XRD patterns of the substrate and superstrate devices just after preparation and after ~800 hours of stressing and the results are shown in **Figure S11**. It can be observed that the perovskite became more crystalline after thermal stressing as reflected by an increase in the intensity of the perovskite peaks at 2Θ ~14^{O} and ~ 28^{O}. We, therefore, speculate that the increase in the FF of the devices after 400 hours may be related to the above-described increase in the crystallinity of the perovskite films. What is also apparent from **Figure S11** is the increase in the intensity of the PbI_2 peak at 2Θ ~12.7^{O} in both the types of devices. Hence, the overall decrease in device performance is most likely related to the degradation of the perovskite.

Conclusion:

In summary, we demonstrated the fabrication of fully vacuum deposited perovskite solar cells in the substrate configuration. A maximum power conversion efficiency (PCE) of ~19%, which is comparable to that of the simultaneously fabricated conventional superstrate cells on ITO-bottom electrode (PCE ~19.5%). Both the substrate and superstrate devices encapsulated with alumina layer exhibited similar thermal stability at 85 ^{O}C in N_2 environment, maintaining > 80% of their original PCE for more than 550 hours. The microstructural analysis of the XRD patterns, as well as, the cross-sectional SEM images of the FAMAPI layers in the two device configurations

revealed different growth and thickness of the simultaneously sublimed perovskite layer in the two cases. Our findings may contribute towards the development of large-area, efficient, and thermally stable fully vacuum-deposited PSCs.

Experimental Procedures:

Resource availability

Lead contact

Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Henk Bolink (henk.bolink@uv.es).

Materials availability

This study did not generate new unique reagents.

Data and code availability

Numerical data and code for optical simulations will be available upon reasonable request.

Vacuum deposition of perovskite layer

The FAMAPI film was grown by co-evaporating PbI_2 and MAI, and FAI. The three precursors are heated in seperate thermally controled crucibles seperated by thermal shields. Upon evaporting the organic amonium salts the chamber pressure temperaray increases due to outgassing but rapidly returns to the base pressure. The evaporation rates of PbI_2 and FAI were monitored using dedicated quartz crystal microbalance (QCMs) sensors close to the PbI_2 and FAI sources and held constant by adjusting their temperature throughout the evaporation process. The evaporation of MAI was controlled using a QCM sensor positioned close to the substrate holder. This QCM sensor had the combined exposure of the fluxes of PbI_2, FAI and MAI, and the optimum value of the measured net rate of their evaporation was also held constant by adjusting the temperature of the MAI's source throughout the evaporation process.

Fabrication of substrate device:

MoO_3/ Ag seed layers and Al bottom electrode were sequentially deposited at the rate of 0.1 Å/s, 0.04 Å/s, and ~0.2 Å/s on cleaned glass substrates. PLD ITO hole extraction layer was deposited by PLD on Al bottom electrode at 0.007 mbar pressure at an O_2: Ar gas ratio of (1:0). All the subsequent layers of the stack from Spiro-TTB to BCP (**Figure 1a**) were grown simultaneously, together with the superstrate device (see also supplemental experimental procedures). The top PLD ITO electrode consisted of a thin, softly deposited ITO buffer layer followed by a thick, harshly depsoited primary ITO layer. The buffer and the primary ITO layers were deposited at 0.042 mbar with O_2: Ar gas ratio of (9:41), and 0.007 mbar pressure with O_2: Ar gas ratio of (1:0), respectively. The top-electrode consisted of a thin (~8 nm) buffer layer of ITO deposited at a relatively high pressure of 0.042 mbar and a primary, thick (~67 nm), dense, and conductive ITO layer deposited subsequently at a low pressure of 0.007 mbar similar to the hole extracting contact (see methods for more details). The 'soft' deposited buffer layer was used to protect the underlying device layers from the 'harsh' deposition of the primary, conductive ITO layer (see **Figure S3**). We highlight that while the ITO layer was required to be deposited twice in the fabrication of the substrate devices, its combined or total thickness was still lower than what is typically needed of the bottom-ITO layers on glass for fabricating superstrate cells. This was followed by the deposition of Ag grids with a thickness of 100 nm around the active cell area. This was done simultaenously with the deposition of the top Ag electrode of the superstrate device. The depsoition of LiF anti reflection layer was also simultaneously done with the superstrate device.

Whole-pattern Le Bail fitting:

The whole-pattern Le Bail fitting of X-ray diffraction patterns was performed using HighScore Plus software.

Optical simulation:

Transfer matrix method based '1-R' simulations were performed using a home-built code integrated with the *tmm* package in a pyhton based IDE. The derivations of the formulas and calculations implemented to develop the *tmm* package can be found here.[29] The values of the optical constants (n,k) of another perovskite composition with similar band-gap as of the FAMAPI layer were used for optical simulation. The optical constants (n,k) of LiF and glass were assumed to be (1.4,0) and (1.5,0) across the spectrum of interest.

Electrical characterization:

Devices were encapsulated with alumina layer deposited by pulsed laser deposition prior to exposure to air and J-V characterization. The active area under illumination for both the superstrate and substrate devices was defined using a shadow mask and had a value of 0.05 cm^2, whereas, the overall active area of the devices or the area considered during the measurement of dark J-V curves, defined as the overlapping area between the top and bottom electrodes, was 0.0825 cm^2. 'The reported efficiencies were obtained from the second or third J-V scan as the efficiency of the devices was found to increase upto the second or third scan.

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Author contribution:

Conceptualization, A.P. and H.J.B.; Methodology, A.P., K.P.S.Z,; Investigation, A.P., C.R.C. M.A.H.F. and H.J.B.; Writing – Original Draft, A.P.; Writing – Review & Editing, H.J.B.; Funding Acquisition, H.J.B. and C.R.C.; Supervision, H.J.B.

Declaration of interests:

The authors declare no competing interests

Supplemental Information:

Supplemental figures: Supplemental Figures S1-S11, Tables S1-S3, Experimental procedures, and References

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Figure captions:

Figure 1. Substrate and superstrate device stack

(A) Schematic od device stacks of p-i-n PSCs in superstrate and substrate configurations

(B) Cross-sectional SEM image of the substrate device. See Also **Figure Sx**

Figure 2. Material properties of perovskite

(A) Absorbance and PL spectra of the FAMAPI perovskite layer on a glass substrate having a 3 nm Spiro-TTB film

(B) X-ray Diffraction pattern of formamidinium methylammonium lead iodide (FAMAPI) perovskite layers in the superstrate and substrate devices. Note that the intensity scale (on y-axis) is the same for both the top and bottom diffractograms. The diffraction peaks originating from the perovskite phase correspond to the same planes in the two FAMAPI layers. The two diffractograms also exhibit a common peak at $2\Theta = 12.6°$ which corresponds to the (001) plane of PbI_2 (denoted by *). The diffraction pattern of the superstrate device exhibits additional peaks at $2\Theta = 30.3°$and 35.2° which correspond to the (222) and (004) planes of crystalline bottom-indium tin oxide (denoted by #), respectively, and at $2\Theta = 38.2°$ which corresponds to the (003) plane of PbI_2 (denoted by |).

Figure 3. Performance of superstrate and substrate PSCs

(A) External Quantum Efficiency (EQE) spectra of the substrate and superstrate devices. The short circuit current density values obtained from the integration of the EQE spectrum and AM 1.5G

photon density spectrum (integrated J_{sc}) for the superstrate and substrate devices are 22.9 and 22.6 mA/cm^2, respectively

(B) Comparison of the EQE spectra of the devices (solid lines) with their simulated 1- device reflectance (1-R, dash-dot lines)

(C) current density-voltage (J-V) curves of the best superstrate and substrate cells measured under simulated AM 1.5G spectrum along with the corresponding PCE parameters obtained in reverse scan

(D) Statistics of the PCE parameters of 26 cells of the two types of devices

Figure 4. Thermal stability of superstrate and substrate PSCs

PCE parameters extracted from the J−V curves taken at different times for the devices kept at 85°C on a hot plate in nitrogen atmosphere.