

Review

Optimizing the Efficiency of Series Resonant Half-Bridge Inverters for Induction Heating Applications

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Abstract: This paper reviews the current state of research on half-bridge (HB) inverters used in induction heating power supplies, emphasizing their topological structures, output power control methods, and switching strategies. The study explores various control techniques to regulate low power levels in a series resonant inverter (SRI) configured with an HB structure for induction heating applications. Pulse frequency modulation (PFM) is commonly employed to regulate standard power levels by adjusting the operating frequency relative to the resonant frequency. As the operating frequency increases beyond resonance, the output power decreases. However, in certain scenarios, achieving low power levels necessitates high frequencies, which introduces significant control challenges. To address these issues, it is crucial to develop alternative approaches that ensure efficient power reduction, without compromising system performance. This work evaluates and compares multiple solutions tailored for a high-frequency induction heating system delivering 18 kW at an operating frequency of approximately 100 kHz. The study places particular emphasis on optimizing key component sizing and analyzing inverter losses to enhance overall system efficiency and reliability.

Keywords: induction heating; resonant converters; SiC power MOSFETs; pulse frequency modulation; pulse density modulation; asymmetrical pulse width modulation; soft switching; high efficiency



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1. Introduction

Induction heating (IH) has gained widespread acceptance in both domestic and industrial applications. In industrial settings, it is predominantly used for heat treatments that require high precision, energy efficiency, and reliable operation, enabling cost-effective and optimized processes. Recent advancements have driven a substantial increase in the use of high-frequency converters for metal heat treatment processes such as surface hardening, brazing, and soldering. This progress has been facilitated by the advent of new semiconductor technologies that improve switching performance and reduce losses using soft-switching techniques [1,2].

In the IH process, the workpiece—the material to be heated—is placed within a magnetic field produced by a coil known as the heating inductor. This coil is powered by an induction heating converter, which delivers a high-amplitude, high-frequency current [3]. Heat is generated in the workpiece through Foucault (eddy) currents induced on its surface, leading to Joule and hysteresis losses. The heated zone's depth, known as the penetration depth (δ), depends on the current frequency, due to the skin effect and the material's heat conduction properties. Higher frequencies result in a shallower penetration depth, while

lower frequencies allow for deeper heating [4]. Figure 1 provides a schematic representation of the electromagnetic principle of IH and highlights the concept of penetration depth.

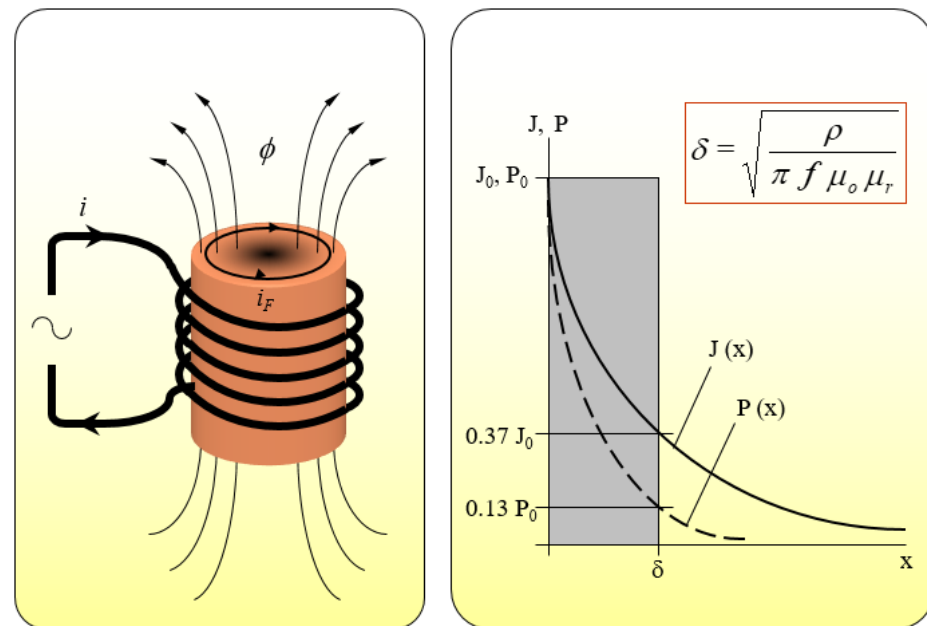


Figure 1. Induction heating and penetration depth, where i is the current of the power supply, i_F is the induced current, ϕ is the magnetic flux, J is the current density, P is the dissipated power, and δ is the penetration depth of a current of frequency f in a material of electrical resistivity ρ and magnetic permeability μ .

The load of an induction heating converter consists of the heating inductor and its equivalent loss resistance, which can be arranged in either a series or parallel configuration, depending on the design. To compensate for the load's reactive energy, a capacitor is included to form a resonant circuit. This capacitor can be connected in series, as in series resonant inverters (SRI) [5–7], or in parallel, as in parallel resonant inverters (PRI) [8–10]. Both inverter configurations are commonly used in applications such as forging, welding, melting, hardening, and other metal heat treatment processes.

In traditional power control schemes, there is a risk of increased switching losses and electromagnetic noise, primarily because switching devices struggle to consistently turn on and off under zero current conditions. As a result, MOSFET inverters are typically favored in high-frequency induction heating applications. However, in high-power industrial applications, IGBTs are often preferred, due to factors such as availability and cost. The use of IGBTs becomes viable if a low-loss power control scheme can be implemented.

Currently, the use of silicon carbide (SiC) MOSFET transistors has enabled the achievement of higher power levels and frequencies. This advancement makes it more feasible to adapt this topology for soft and medium industrial heating applications, ensuring improved efficiency.

Figure 2 illustrates the primary power conversion scheme commonly found in single-coil induction heating (IH) systems. The system starts with an electromagnetic compatibility (EMC) filter to ensure the power converter meets electromagnetic standards. An AC-DC converter then generates a DC-bus that supplies power to the inverter block. The rectifier stage can be either uncontrolled, such as a diode rectifier, or controlled, depending on the system's requirements.



Figure 2. Schematic diagram of an IH generator [1].

The controlled rectifier implementation provides an additional degree of freedom for the control system. It can be realized either as a controlled rectifier [11] or as a combination of a diode rectifier and a DC-DC converter [12]. This controlled rectifier configuration enhances the flexibility of the IH system's control, allowing for more sophisticated adjustments and optimizations in the power conversion process.

The DC-AC power converter, commonly referred to as the inverter, is a crucial component responsible for supplying medium-frequency currents to energize the inductor [13]. The operating frequency typically exceeds 20 kHz, to prevent audible noise, reaching up to 1 MHz depending on the specific application. Presently, many IH systems adopt either voltage source or current source resonant inverters [14] to achieve efficient and high-power-density implementations.

Regarding the inverter topology, there are two main types: the full-bridge (FB) inverter and the half-bridge (HB) inverter. When applied to series resonant circuits, a full-bridge series resonant inverter (FB-SRI) features four switches, producing a square wave (SW) output with an amplitude equal to the input voltage. In contrast, a half-bridge series resonant inverter (HB-SRI) uses only two transistors, and the SW output has an amplitude equal to half the input voltage. The HB-SRI topology is the most widely adopted solution for domestic and light industrial applications, due to its simplicity, high efficiency, and cost-effectiveness [15,16].

In device selection, the balance between cost and performance is as important as the electrical parameters and efficiency values. The introduction of SiC MOSFET transistors has further enhanced the power and frequency capabilities of this topology, allowing it to be adapted for industrial heating applications, with excellent efficiency [17,18]. These improvements are critical to ensuring system reliability, maximizing output power, and minimizing the size and cost of heat sinks. Despite the cost disadvantage, the use of SiC power devices is increasing in industrial applications [19,20].

Traditional SW modulation remains a common technique for power regulation in HB-SRI for induction heating applications. Power control is typically achieved using pulse frequency modulation (PFM), operating above the resonant frequency to maintain zero voltage switching (ZVS) conditions [5,6]. However, as the frequency and phase of turn-off transitions increase to reduce power, the inverter's efficiency decreases. To address this, pulse density modulation (PDM) has been proposed to improve efficiency [21,22], but it faces challenges at medium and low power levels.

Variable frequency asymmetrical pulse-width modulation (APWM) offers a generalized approach, combining SW modulation and classical asymmetrical duty cycle control methods [7,23]. With APWM, modulation parameters include both switching frequency and duty cycle, enabling power regulation with minimal frequency variation and reduced power losses. APWM serves as an alternative to phase-shift (PS) modulation, commonly used in full-bridge inverters but unsuitable for HB configurations [24].

Industrial induction heating applications often require a high current to flow through the heating inductor, which necessitates the use of a current step-up transformer connected to the inverter's output. If the inverter's output contains a DC voltage component, the transformer's magnetic material may saturate, causing significant overcurrents in the

inverter. This paper explores potential control strategies to eliminate the DC voltage component, while also ensuring an optimal balance of power losses in the inverter switches. For this purpose, enhanced asymmetrical pulse width modulation (EAPWM) and enhanced pulse density modulation (EPDM) will be introduced, which include novel modifications to traditional modulation techniques [25,26].

The structure of the paper is as follows: Section 2 describes the materials and methods, focusing on the configuration of the HB-SRI converter, the analysis of the converter using traditional modulation techniques, and the introduction of novel techniques, EAPWM and EPDM. Section 3 presents the results of the review, including a comprehensive loss analysis of the HB-SRI converter and a comparative study of the performance of each modulation technique in terms of efficiency and frequency variation during output power regulation. Experimental data are also used to validate the results. Finally, the conclusions are presented.

2. Materials and Methods

2.1. Converter Configuration

Figure 3 shows a simplified schematic of the converter. The output power stage consists of a voltage-fed HB inverter using two SiC MOSFET transistors Q_1 - Q_2 and two high-frequency capacitors C_3 - C_4 that play the role of filter capacitors at the input of the half-bridge resonant inverter, necessary to close the high-frequency component of the current through the reverse diodes. A series resonant circuit is connected to the inverter output. This resonant circuit is composed of the resonant capacitor C , the induction heating coil L , and the equivalent series resistance R [16,27]. The input impedance $Z(\omega)$ is

$$Z(\omega) = R + i \left(L\omega + \frac{1}{C\omega} \right) = L \left[\frac{\omega_0}{Q} + i \left(\frac{\omega^2 - \omega_0^2}{\omega} \right) \right], \quad (1)$$

where the resonant quality factor Q is defined by

$$Q = \frac{L\omega_0}{R}, \quad (2)$$

and ω_0 is the resonant angular frequency given by

$$\omega_0 = \frac{1}{\sqrt{LC}}. \quad (3)$$

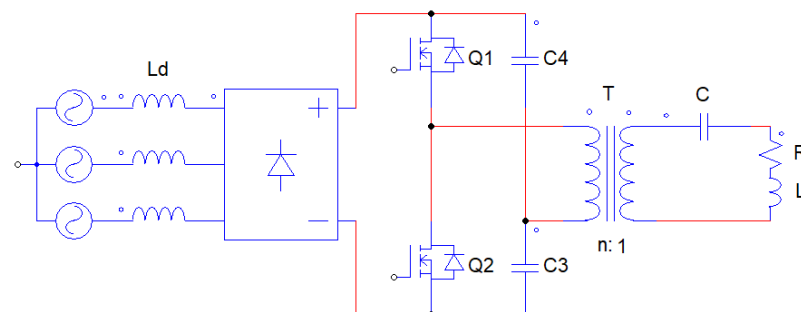


Figure 3. System configuration.

Since a heating inductor in industrial induction applications requires high current, the converter uses a matching transformer T to boost the current and to adapt the impedance of the load circuit. The inverter's DC power supply is derived from a three-phase diode bridge rectifier, which is connected to the 400 V, 50 Hz mains supply through inductors L_d

of 100 μH , which improves the line current distortion [28,29]. For the application chosen for this paper, the nominal output power is 18 kW and the working frequency is 100 kHz. The required heating coil for the application is a 3 turns inductor of 2 μH , with a quality factor Q of 10. The transformer ratio n is 5. Table 1 shows a resume of the main specifications.

Table 1. Converter specifications.

Component	Symbol	Value	Unit
Nominal Output Power	P_o	18	kW
Nominal Frequency	f_o	100	kHz
DC Input Voltage	V_d	540	V
Resonant Inductor	L	2	μH
Output Quality Factor	Q	10	
Transformer Ratio	n	5	
Resonant Capacitor	C	1.27	μF
Equivalent Series Resistor	R	126	$\text{m}\Omega$

The phase α of the resonant circuit impedance, hence, the phase between the output current and output voltage at the working frequency is

$$\alpha = \arg(Z(\omega)) = \arctan\left(Q\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)\right), \quad (4)$$

and the module of the impedance can be expressed by

$$|Z(\omega)| = \left| R + jL\omega + \frac{1}{jC\omega} \right| = \frac{R}{\cos \alpha}. \quad (5)$$

Figure 4 shows a graphical representation of the module and the argument of the resonant circuit impedance. To meet the zero-voltage switching (ZVS) condition of the HB-SRI, we must ensure that the current is always negative or zero when the transistors switch when the current flows through the freewheeling diode. This means that the phase angle α must always be zero or positive, and therefore, the operating frequency must always be greater than or equal to the resonant frequency. This allows us to define two frequency zones in Figure 4: the permissible zone, shaded in green, and the prohibited zone, shaded in red.

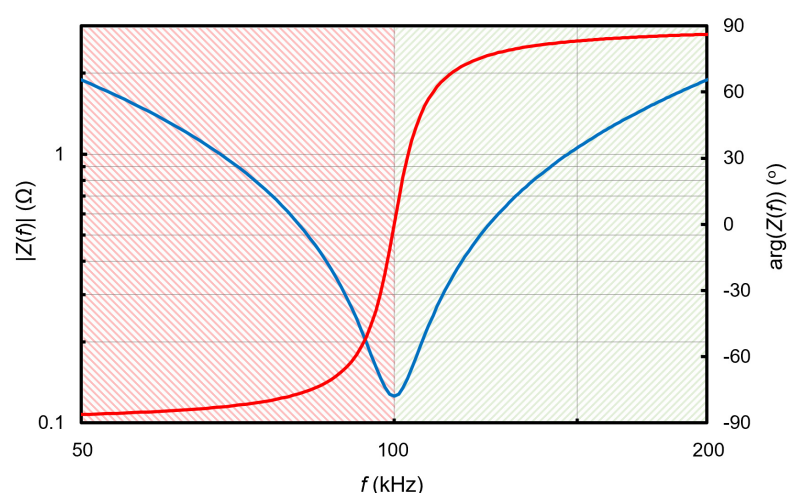


Figure 4. Phase and module impedance of the HB-SRI circuit.

Table 1 shows a resume of the main specifications of the converter and its components.

Figure 5 shows simplified schematics of a HB SRI composed by MOSFET transistors Q_1 - Q_2 , their free-wheeling diodes D_1 - D_2 , and two high-frequency capacitors C_3 - C_4 that allow the flow of circulating current. C_1 - C_2 represent the equivalent capacitance of the inverter switches, including the snubber capacitor and the output capacitance of the MOSFETs. Note that the transformer T present in Figure 3 has been removed and, hence, the impedances of the resonant circuit corresponding to C , L , and R , have been transformed by the turn's ratio n . The inverter is fed with the direct voltage V_d that comes from the input rectifier.

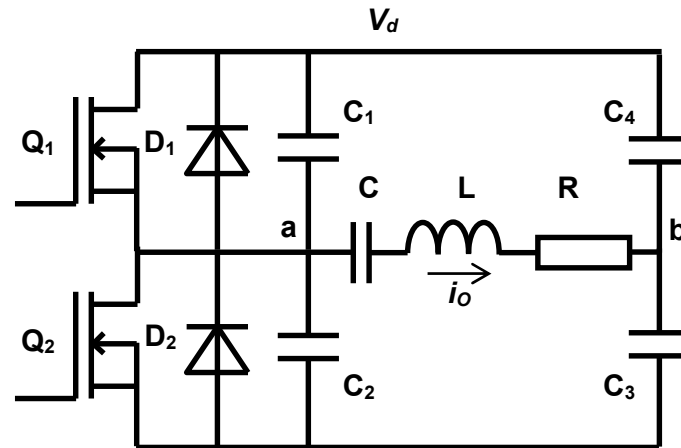


Figure 5. HB-SRI circuit.

From this simplified circuit, the design equations and switching sequences will be derived by applying the various power control techniques explained below.

2.2. Control by Pulse Frequency Modulation (PFM)

Figure 6 shows the simplified output voltage and current waveforms of the PFM HB-SRI inverter, assuming a relatively high value of the quality factor Q , which allows us to consider that the output current of the inverter is sinusoidal for any value of operating frequency. When a PFM is used, transistors Q_1 and Q_2 operate with a quasi-complementary duty cycle of 0.5, with the exception of dead time that determines the phase β where the output voltage is changing from positive to negative and the output current is still positive. A mathematical expression for the minimum values of β required to achieve ZVS is derived from the following charge analysis [30]. The current in the resonant circuit must be sufficient to change the voltage across the switching capacitor $C_S = C_1 + C_2$ up to $V_d/2$ (or $-V_d/2$) in the time β_{min}/ω just before the output current crosses zero. From these charge relations, β_{min} can be calculated as

$$\beta_{min} = \cos^{-1} \left(1 - \frac{\omega C_S V_d}{I_C} \right), \quad (6)$$

where I_C is the switching current I_{CQ1} or I_{CQ2} . The phase β_{min} determines the minimum dead time between the transistors of the HB-SRI. The dead time must be calculated continuously using the parameters of the resonant circuit, including the resonant frequency, the load conditions, and the required phase shift to ensure ZVS using (6) with sufficient safety margin. In practice, it is adjusted by $\beta = 1.1 \beta_{min}$. Excessive dead time can lead to a reduction in power transfer efficiency and an increase in harmonic distortion.

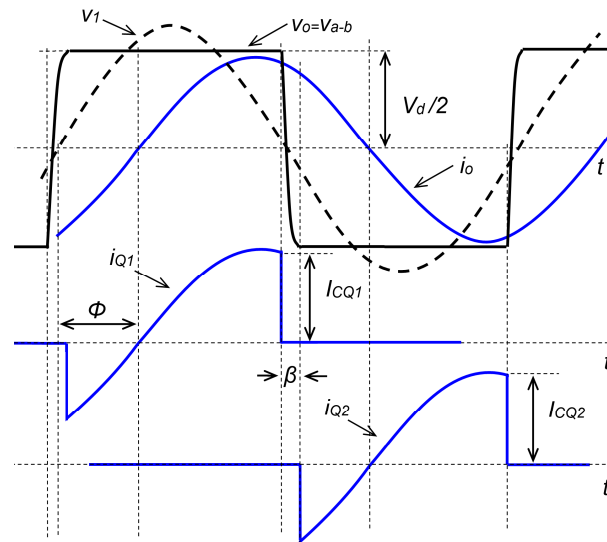


Figure 6. Simplified output voltage and current waveforms in PFM HB-SRI.

The resulting voltage across the resonant circuit between points *a* and *b* (Figure 4) is a quasi-square wave v_o whose first harmonic has an amplitude V_o given by

$$V_o = \frac{4V_d}{\pi\beta} \cos \frac{\beta}{2} \sin \frac{\beta}{2} = \frac{2V_d}{\pi\beta} \sin \beta, \quad (7)$$

where V_d is the average value of the DC-link voltage.

The output power of the inverter is regulated by varying its operating frequency above the resonant frequency, which causes a phase shift between the output voltage and current. Then the amplitude of the output current is

$$I_o = \frac{2V_d}{\pi\beta n^2 R} \cos \varphi \sin \beta, \quad (8)$$

therefore, the output power is

$$P = \frac{2V_d^2}{\pi^2 \beta^2 n^2 R} \cos^2 \varphi \sin^2 \beta. \quad (9)$$

The current of the high side and low side switches are i_{Q1} and i_{Q2} , respectively. The turn-off switching currents I_{CQ1} and I_{CQ2} are the same and depend directly on the phase shift, which is always positive, ensuring ZVS operation.

$$I_{CQ1} = I_{CQ2} = I_{CQ} \approx I_o \sin \left(\phi + \frac{\beta}{2} \right). \quad (10)$$

Assuming that the value of the phase β is small compared to the current period, we can obtain the following approximation in calculating the RMS (root mean square) values of the currents for each switch.

$$I_{Q1} = I_{Q2} = I_Q \approx \frac{I_o}{2}. \quad (11)$$

Figure 7 shows the complete switching sequence of the frequency modulation PFM applied to a HB-SRI inverter organized in two columns. The top of each column shows the simulated waveforms of the inverter output voltage v_o , the output current i_o , and the two gate trigger signals of the transistors vg_1 and vg_2 . The switching sequence steps are labeled with numbers, and the corresponding inverter schematics for each step are shown

below. In these schematics, current-carrying devices are represented by solid lines, while voltage-blocking devices are indicated by dotted lines. Arrows and $\pm$ signs are used to illustrate the direction of the current and the polarity of the voltage at the conclusion of each step. The first switching process, in the time interval 2, is the turn-off of Q_1 , which is carried out with a switching current determined by the phase $\beta + \phi$. The next switching, in the time interval 6, is the turn-off of Q_2 which is carried out in similar conditions.

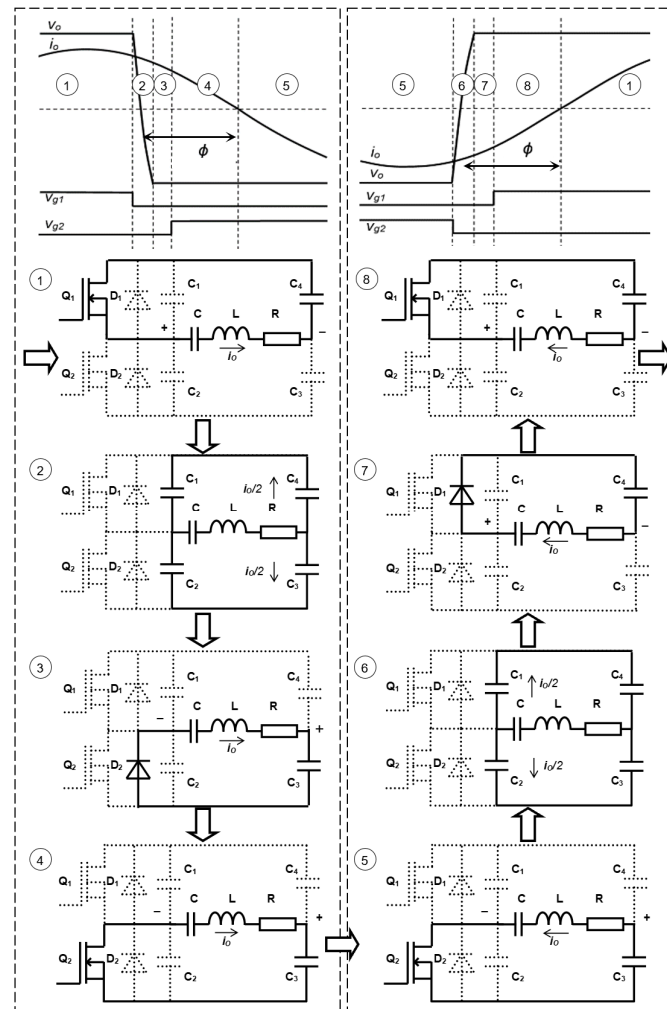


Figure 7. Complete switching sequence of the PFM HB-SRI.

With a careful system for generating the gate signals of the transistors, it is possible to ensure that the output voltage applied to the output transformer of the PFM HB-SRI has a zero average value and, therefore, a DC blocking capacitor is not required to prevent magnetic saturation of the transformer, resulting in savings in the cost and volume/weight of the inverter.

The control circuit designed to implement the PFM HB-SRI is a load-adaptive variable-frequency system [31,32] capable of regulating the output power. Figure 8 presents the block diagram of the proposed control circuit. The signal V_f is fed into the PFM modulator to determine the operating frequency f , which enables power regulation. Since the phase detector and the VCO function as a phase-locked loop (PLL), the signal Q attempts to remain in phase with the inverter output current i_o , thereby limiting the minimum operating frequency. The TD1 block delays the Q signal to ensure the ZVS condition. The dead time represents the time interval between the turn-off and turn-on of the transistors. The dead time control circuit includes two programmable delay blocks, TD2 and TD3, which

generate the reference signal for turning off all the inverter transistors, considering the calculation outlined in Equation (6).

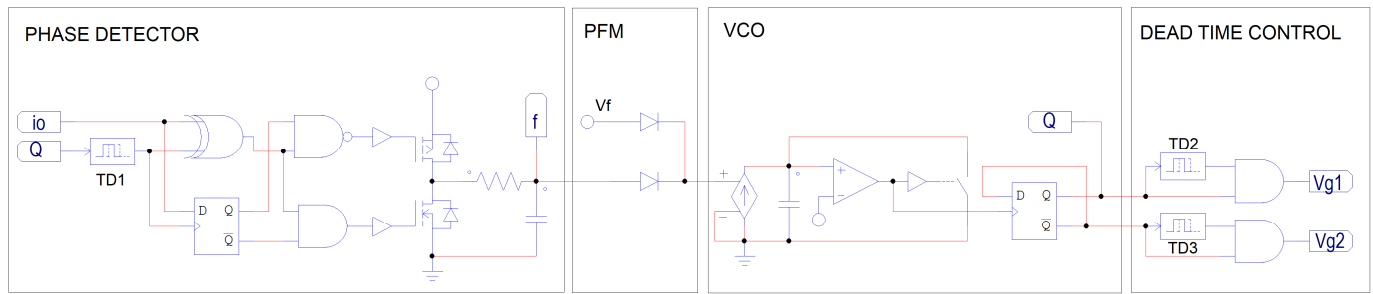


Figure 8. Control block diagram of the PFM HB-SRI.

2.3. Control by Asymmetrical Pulse Width Modulation (APWM)

Figure 9 illustrates the simplified output voltage and current waveforms of the inverter when asymmetrical pulse width modulation (APWM) [33] is applied. In this modulation scheme, Q_1 represents the high-side transistor of the inverter, which turns off before the zero crossing of the output current. Q_2 is the low-side transistor, and the conduction cycles of Q_1 and Q_2 are complementary. The inverter's output power is regulated by adjusting the duty cycle of Q_1 and Q_2 , which introduces a phase shift between the output voltage and current. Note that the switching current I_{CQ1} is always low and only i_{Q2} presents a high value of the switching current I_{CQ2} .

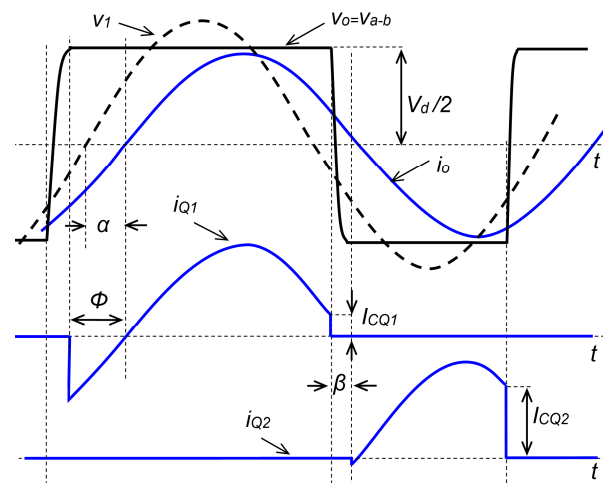


Figure 9. Simplified output voltage and current waveforms in APWM HB-SRI.

In the APWM HB-SRI, the expression to calculate the amplitude of the first harmonic of v_o is

$$V_1 = \frac{4V_d}{\pi\beta} \cos\left(\frac{\varphi + \beta}{2}\right) \sin\frac{\beta}{2}. \quad (12)$$

As the value of α is approximately equal to $(\varphi + \beta)/2$, then the amplitude of the output current is given by

$$I_o = \frac{4V_d}{\pi\beta n^2 R} \cos^2\left(\frac{\varphi + \beta}{2}\right) \sin\frac{\beta}{2}, \quad (13)$$

therefore, the output power is

$$P = \frac{8V_d^2}{\pi^2\beta^2 n^2 R} \cos^4\left(\frac{\varphi + \beta}{2}\right) \sin^2\frac{\beta}{2}. \quad (14)$$

In this case, the switching currents of each switch are different and can be calculated with

$$I_{CQ1} = I_o \sin \beta \quad (15)$$

and

$$I_{CQ2} = I_o \sin(\phi + \beta). \quad (16)$$

The RMS currents of each switch are obtained through the following approximations:

$$I_{Q1} \approx \sqrt{\frac{1}{2\pi} \int_{-\phi}^{\pi} (I_o \sin(\omega t))^2 d(\omega t)} = \frac{I_o}{2\sqrt{\pi}} \sqrt{\pi + \phi - \frac{\sin 2\phi}{2}} \quad (17)$$

and

$$I_{Q2} \approx \sqrt{\frac{1}{2\pi} \int_{-\pi}^{-\phi} (I_o \sin(\omega t))^2 d(\omega t)} = \frac{I_o}{2\sqrt{\pi}} \sqrt{\pi - \phi + \frac{\sin 2\phi}{2}}. \quad (18)$$

Figure 10 shows the complete switching sequence of the asymmetrical pulse width modulation APWM applied to a HB-SRI inverter. The turn-off of Q_1 is carried out with a relatively small switching current determined by the phase β that ensures the ZVS condition. The next switching, in the time interval 6, is the turn-off of Q_2 , which is performed with a much larger switching current determined by phase ϕ .

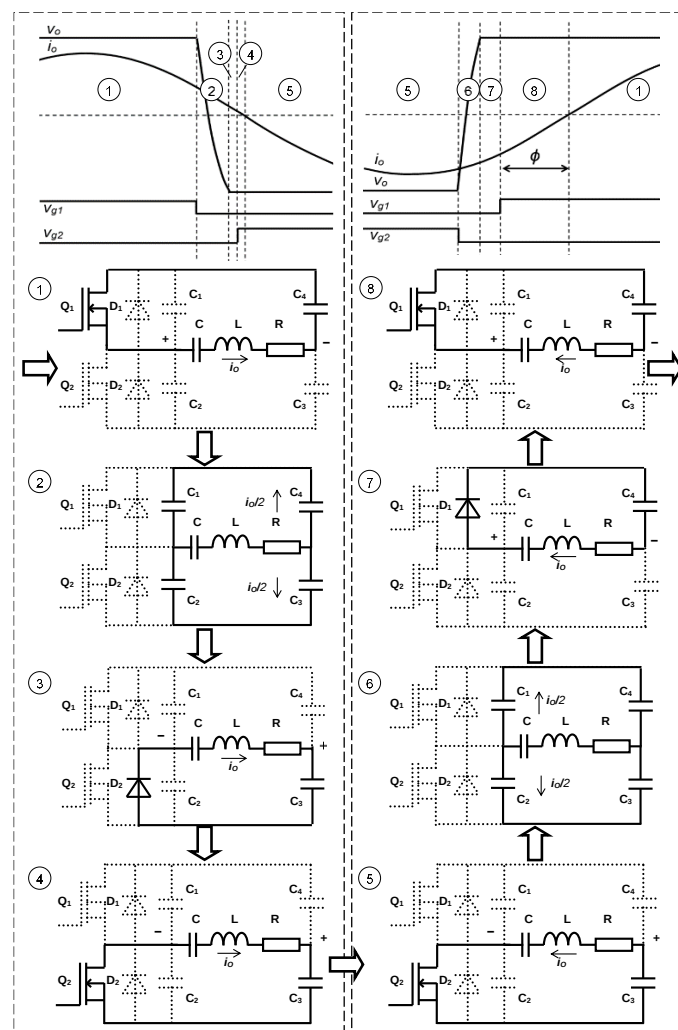


Figure 10. Complete switching sequence of the APWM HB-SRI.

2.4. Control by Enhanced Asymmetrical Pulse Width Modulation (EAPWM)

The previous paragraphs described the operation of the APWM HB-SRI, where the losses of Q_2 are greater than those of Q_1 and a large DC voltage can be applied to the transformer. To prevent this without the need to include a blocking capacitor and to also achieve proper equalization in the transistor losses, EAPWM control [25] can be used. To implement this solution, it is necessary to extend the switching cycle of the standard APWM control by alternately changing the switching conditions of Q_1 and Q_2 from cycle to cycle. This would allow the higher power losses to be alternately dissipated by Q_1 in one cycle and by Q_2 in the next cycle, while nullifying the average output voltage.

In this situation, the current through each switch will also be balanced. In this case, the following expressions allow calculating the equivalent RMS currents of each switch.

$$I_Q = \frac{I_{Q1} + I_{Q2}}{2} \approx \frac{I_o}{4\sqrt{\pi}} \left(\sqrt{\pi + \phi - \frac{\sin 2\phi}{2}} + \sqrt{\pi - \phi + \frac{\sin 2\phi}{2}} \right). \quad (19)$$

The control circuit designed to implement the EAPWM is a load-adaptive variable frequency system. It is designed to ensure zero voltage switching (ZVS) under all operating conditions and to generate the switching sequence described earlier. This adaptive control optimizes power regulation, while maintaining efficient and reliable inverter operation. Figure 11 shows the block diagram of the proposed control circuit. Since the phase detector and the VCO act like a phase-locked loop (PLL), the signal Q will be in phase with the inverter output current i_o . This square signal determines the rising slope of the trigger signal of the high side of the inverter near the zero crossing of the current. The signal V_c inputs the EAPWM modulator to generate the rectangular signal that defines the phase ϕ that allows the power regulation.

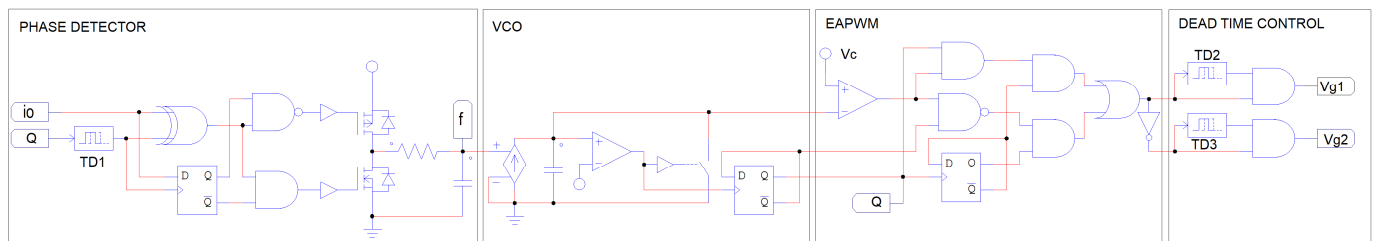


Figure 11. Control block diagram of the EAPWM HB-SRI.

The Figure 12 shows the simulation results of the EAPWM HB-SRI, displaying the output voltage v_o and the output current i_o . The use of this modulation, where the switching conditions of Q_1 and Q_2 are alternately exchanged, ensures that the average value of the output voltage is zero.

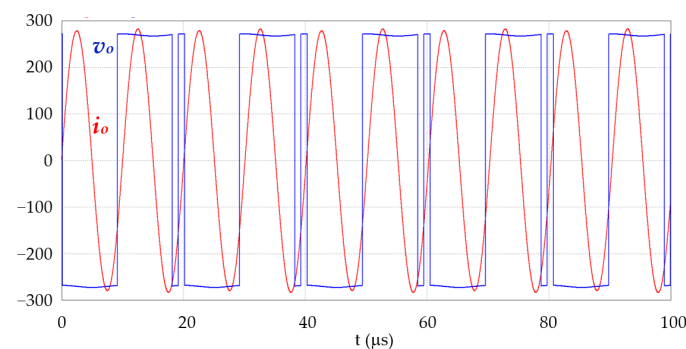


Figure 12. Simulation of the EAPWM HB-SRI. Inverter output voltage (blue) in V and current (red) in A.

2.5. Control by Pulse Density Modulation (PDM)

When pulse density modulation (PDM) is used, the HB-SRI operates in two modes. In active mode, the inverter behaves as a square wave voltage source with an amplitude of $V_d/2$ for several resonant cycles. In passive mode, it acts as a zero-voltage source for a few cycles. The alternating pattern of these modes defines a period T , which is an integer multiple of the switching period T_s . The RMS value of the output voltage is directly proportional to the pulse density m , defined as the ratio of the active mode duration T_{on} to the total period T of the PDM cycle. To maximize inverter efficiency, the phase difference between the voltage and output current in active mode should be minimized, constrained by the phase β , as described in Equation (6).

Figure 13 displays the simplified output voltage and current waveforms of the inverter during the active mode of the PDM.

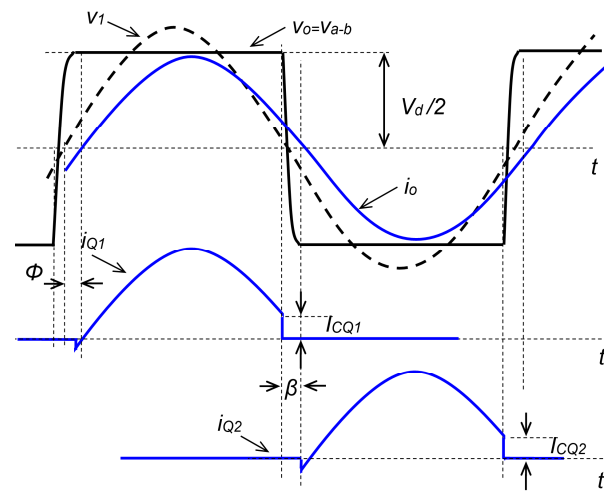


Figure 13. Simplified output voltage and current waveforms in PDM HB-SRI in active mode.

In the active mode of the PDM HB-SRI, the amplitude of the first harmonic of v_o is

$$V_1 = \frac{2V_d}{\pi\beta} \sin \beta. \quad (20)$$

By approximating ϕ as $\beta/2$, the amplitude of the output current in the active mode is given by

$$I_o = \frac{2V_d}{\pi\beta n^2 R} \cos \frac{\beta}{2} \sin \beta. \quad (21)$$

Taking into account the pulse density m , the output power is

$$P = m \frac{2V_d^2}{\pi^2 \beta^2 n^2 R} \cos^2 \frac{\beta}{2} \sin^2 \beta \quad (22)$$

In this case, the switching current of each switch is

$$I_{CQ1} = I_{CQ2} = I_{CQ} = I_o \sin \beta \quad (23)$$

Figure 14 shows the switching sequence of the pulse density modulation PDM in the active mode applied to an HB-SRI inverter. The turn-off of Q_1 and Q_2 is carried out with a relatively small switching current determined by the phase β that ensures the ZVS condition.

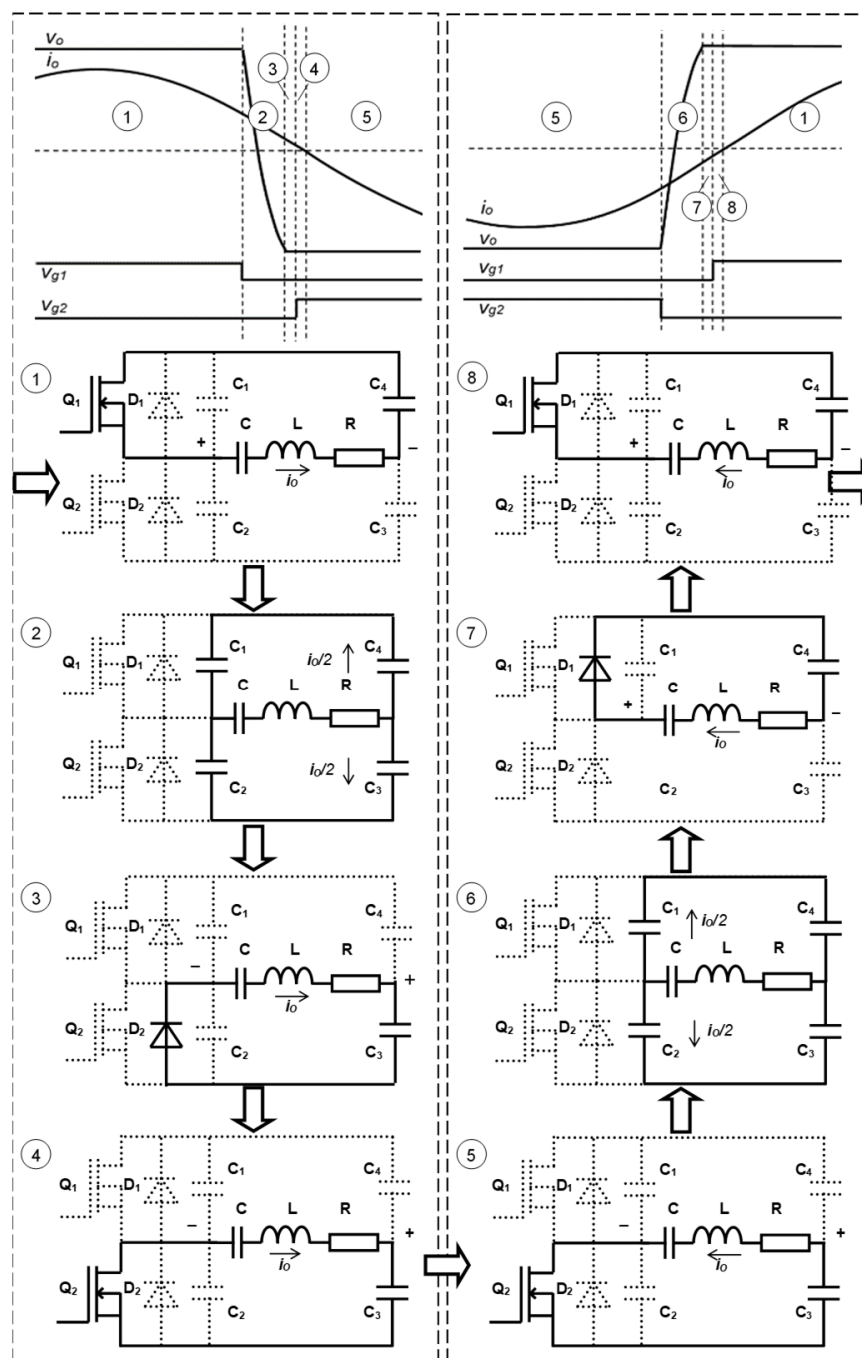


Figure 14. Complete switching sequence of the PDM HB-SRI in active mode.

After the last switching operation performed in active mode, the passive mode of PDM modulation begins, where no further switching occurs. The gate signals of each switch remain unchanged, allowing the free flow of current through the resonant circuit. This current flows through the active switch and the capacitor opposite it until the first switching operation in active mode begins.

Figure 15 shows the simplified output voltage and current waveforms of the inverter in the passive mode of the PDM after an inverter switch from negative to positive voltage (a) and a switch in the reverse direction (b). Figure 16 shows the switching sequences of the pulse density modulation PDM in the passive mode applied to a HB-SRI inverter corresponding to cases (a) and (b) of Figure 15, respectively.

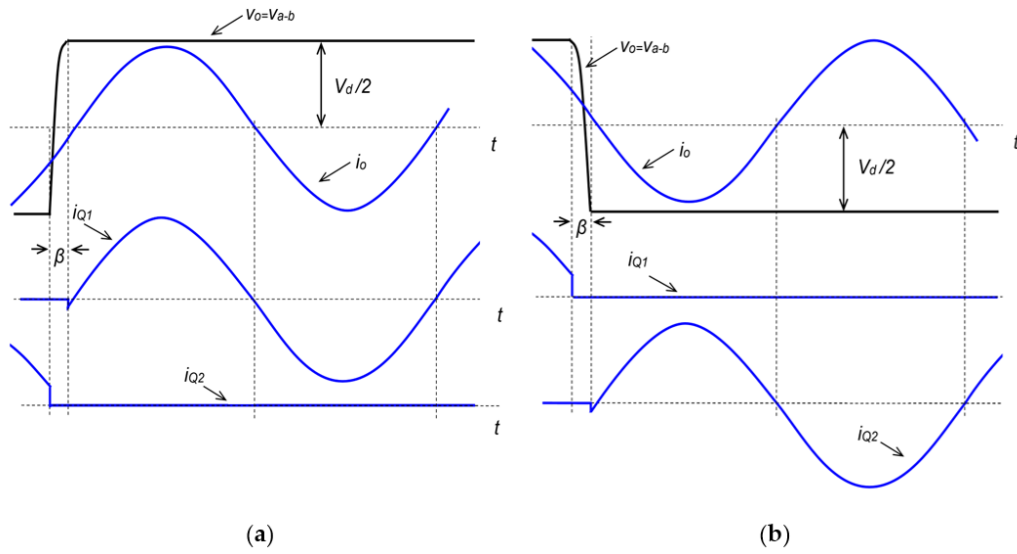


Figure 15. Simplified output voltage and current waveforms in PDM HB-SRI in passive mode when inverter switches from negative to positive voltage (a) and in the reverse way (b).

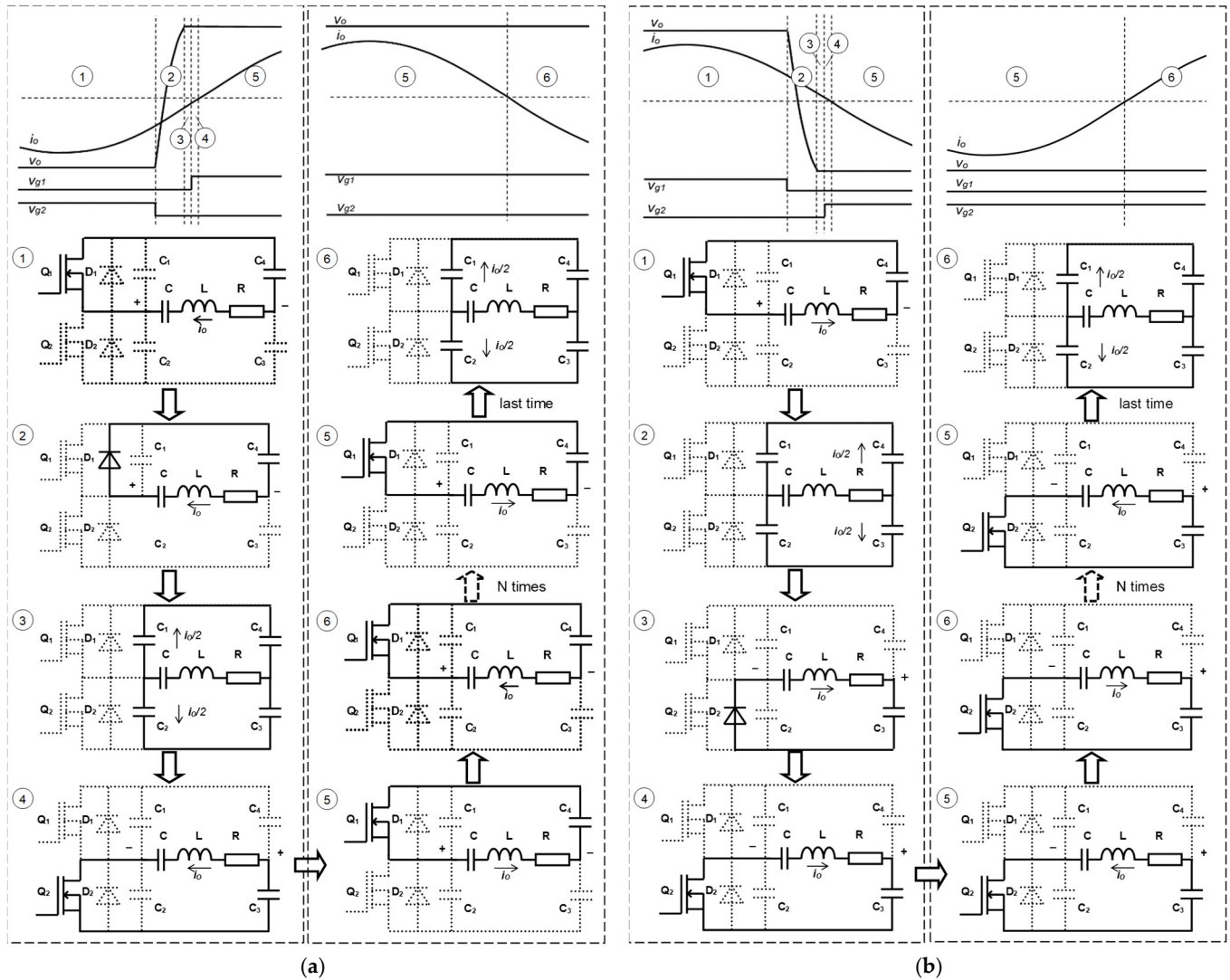


Figure 16. Complete switching sequences of the PDM HB-SRI in passive mode when inverter switches from negative to positive voltage (a) and in the reverse way (b).

2.6. Control by Enhanced Pulse Density Modulation (EPDM)

It can be observed that the average value of the inverter's output voltage is zero in active mode, while in passive mode, the value depends on the relative duration of the previously described passive modes (a) and (b). If an appropriate inverter power control system, named enhanced pulse density modulation (EPDM), ensures that this relative duration is balanced, the DC value of the inverter's output voltage will be cancelled, and the current through each switch will also be balanced. In this case, the following expressions allow calculating the RMS currents of each switch.

$$I_{Q1} = I_{Q2} = I_Q \approx \sqrt{m} \frac{I_o}{2} \quad (24)$$

Figure 17 shows the block diagram of the proposed control circuit. The signal T and Ton inputs the EPDM modulator to define the modulator period and the duration of the active mode, respectively. A logic circuit is included to balance the DC of the output voltage, changing alternatively the passive modes (a) and (b). Since the phase detector and the VCO act like a phase-locked loop (PLL), the signal Q will be in phase with the inverter output current i_o , and the block TD1 delays the Q signal to ensure the ZVS condition. Two programmable delays, TD2 and TD3, adjust the dead times.

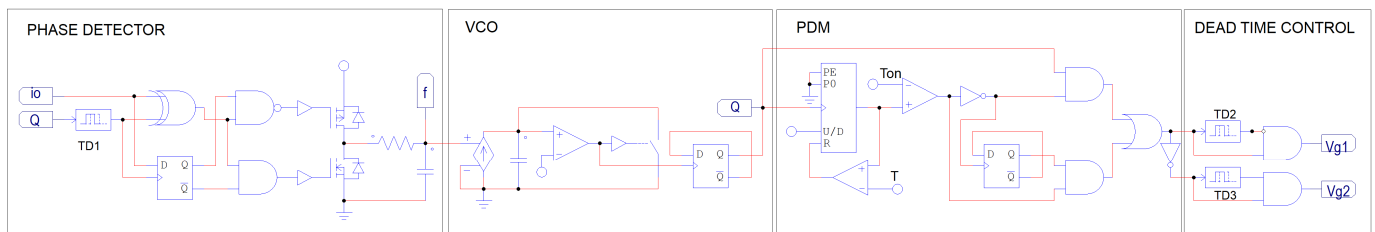


Figure 17. Control block diagram of the EPDM HB-SRI.

The Figure 18 shows the simulation results of the EPDM HB-SRI, displaying the output voltage v_o and the output current i_o . The use of this modulation, where the active modes are alternately exchanged, ensures that the average value of the output voltage is zero.

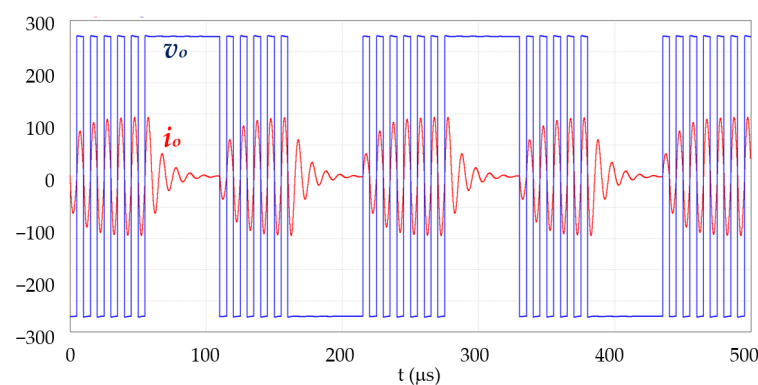


Figure 18. Simulation of the EPDM HB-SRI. Inverter output voltage (blue) in V and current (red) in A.

3. Results

3.1. Power Losses Analysis

In this subsection, the power losses of the HB-SRI will be calculated using the PFM, EAPWM, and EPDM modulation schemes discussed earlier. The power loss analysis considers only the contributions from conduction losses (P_{CD}) and switching losses (P_{SW})

of the transistors [34]. The analysis of P_{SW} focuses specifically on the turn-off losses of the inverter bridge transistors, as the turn-on losses are negligible due to the ZVS condition.

The inverter is a HB that uses only one unit for each switch. The transistors chosen are the SiC MOSFET C3M0032120K of $V_{DS} = 1200$ V and $R_{DSon} = 32$ m Ω .

Considering that both positive and negative currents flow through the resistive channel of the transistor, there are not significant losses in the diodes and the conduction losses for each transistor can be calculated only using (15).

$$P_{CD} = I_Q^2 R_{DSon}. \quad (25)$$

Note that the RMS current of the transistor is different for each modulation, having to use (11) for PFM, (19) for EPWM, and (24) for EPDM.

On the other hand, the switching power losses of each transistor can be calculated using on the graphs of the turn-off switching energy E_{OFF} provided by the manufacturer, using the following polynomial function:

$$E_{OFF} = a I_{CQ}^2 + b I_{CQ} + c, \quad (26)$$

where a , b , and c take the values of Table 2.

Table 2. Coefficients of second order polynomial function.

Magnitude	Symbol	Value	Unit
Second order coefficient	a	0.0546	$\mu\text{J}\text{A}^{-1/2}$
First order coefficient	b	-1.7479	$\mu\text{J}\text{A}^{-1}$
Constant term	c	37.8	μJ

In (26), I_{CQ} represents the switch current of each transistor taking different values for each type of modulation, using (10) for PFM and (23) for EPDM. In these cases, the switching turn-off losses of each transistor can be calculated with

$$P_{SW} = E_{OFF} f. \quad (27)$$

For the EAPWM, two switching currents given by (15) and (16) must be used, and then the switching turn-off losses of each transistor can be calculated with

$$P_{SW} = \frac{E_{OFFQ1} + E_{OFFQ2}}{2} f. \quad (28)$$

Since the inverter has of two transistors, the total power losses are calculated using the following equation:

$$P_{TOT} = 2P_{CD} + 2P_{SW}. \quad (29)$$

For the efficiency calculation, the losses in the high-frequency transformer, capacitors, heating inductor, and all power connections and auxiliary circuits were not taken into account. Therefore, the efficiency of the inverter can be calculated using the following equation:

$$\eta = \frac{P}{P + P_{TOT}}. \quad (30)$$

3.2. Comparative Study

In this subsection, the performance of the three modulations discussed in the previous sections is compared. The primary parameter under consideration is the efficiency of the inverter, accounting solely for the losses in the transistors that comprise it. Figure 19

illustrates the result of (30) for PFM (red), EAPWM (blue), and EPDM (green) as a function of the output power normalized to its maximum value.

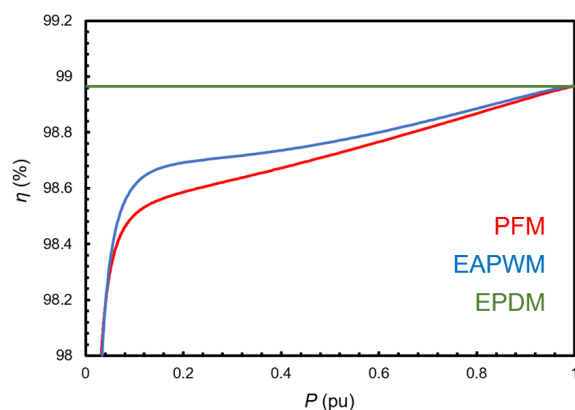


Figure 19. Calculated efficiency of HB-SRI inverter for different modulations in function of normalized output power.

It is observed that the best modulation is EPDM, where both the power losses and the output power are directly proportional to the modulation density m , and therefore, the efficiency remains constant. On the other hand, it is observed that the least efficient modulation is PFM, which is penalized by the increase in losses in the two switches of the inverter as the phase between the voltage and the output current increases. Therefore, pulse frequency modulation (PFM) is not a preferable solution for low power regulation, especially in high-frequency operation.

The efficiency of EAPWM modulation occupies an intermediate position, since it only experiences significant losses alternately in a single switch. Note that the efficiency of the three modulations coincides at the maximum of the inverter, as in this situation the switching conditions are the same. The maximum efficiency achieved was over 98.9%.

Another parameter that should be considered in this comparative study is the variation in the operating frequency when regulating the output power. The ideal situation is one in which the frequency remains unchanged in any case. Any variation in frequency is important when applying filtering or measurement techniques, and it also has some impact on the quality of certain thermal treatments performed by induction heating. Figure 20 shows a representation of the variation in the operating frequency normalized to the resonance frequency value for different output power values.

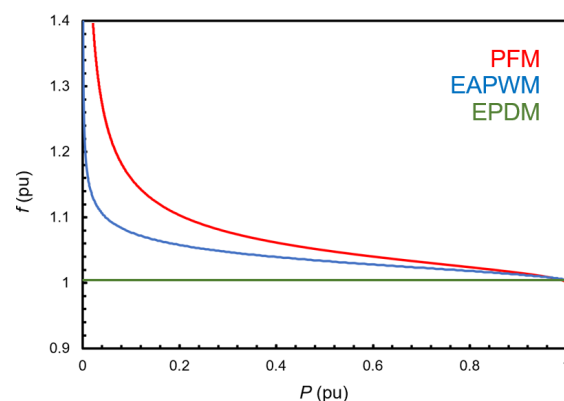


Figure 20. Normalized operating frequency of HB-SRI inverter for different modulations as a function of normalized output power.

It is observed that, once again, the best modulation is EPDM, where the operating frequency remains constant, while PFM shows the worst behavior. EAPWM modulation maintains an intermediate performance.

Since the efficiency at maximum output power is the same in each case, and therefore the maximum power losses are also the same, a single calculation of the maximum temperature of the transistor's junction can be performed for the three modulations. This junction temperature can be calculated using the following expression:

$$T_{Jmax} = P_{max}(R_{thJC} + R_{thCH} + R_{thHA}) + T_A \quad (31)$$

where P_{max} is the maximum power loss of a transistor. It is important to ensure that the junction temperature of the transistors T_{Jmax} does not exceed the maximum allowed limit of 175 °C under the worst-case condition. Table 3 shows the parameters and results of the thermal analysis.

Table 3. Parameters and results of the thermal analysis.

Magnitude	Symbol	Value	Unit
Maximum power loss per transistor	P_{max}	94.6	W
Thermal resistance junction to case	R_{thJC}	0.44	K/W
Thermal resistance case to heatsink	R_{thCH}	0.2	K/W
Thermal resistance heatsink to ambient	R_{thHA}	0.3	K/W
Ambient temperature	T_A	40	°C
Maximum junction temperature	T_{Jmax}	124.2	°C

3.3. Experimental Results

This subsection presents the experimental results obtained from testing an 18 kW power prototype operating at a frequency of 100 kHz. The inverter was powered by a 540 V DC voltage source. The component values of the resonant circuit were those determined in the previous sections. For the experimental verification, a test bed was constructed, consisting of the following components:

- A complete induction heating (A) converter that contained a HB-SRI inverter with two C3M0032120K SiC MOSFETs and four film capacitors of 33 μ F, an input three phases rectifier, and an integrated digital electronic control on an FPGA-based system mounted on a water cooling heatsink.
- An output transformer (B) with $n = 5:1$
- Two high-power capacitors (C) of 2.5 μ F connected in series, usable for induction heating.
- A solenoidal heating inductor (D) of 2 μ H.
- A test load (E).

Figure 21 shows the test bed used to obtain the following experimental results.

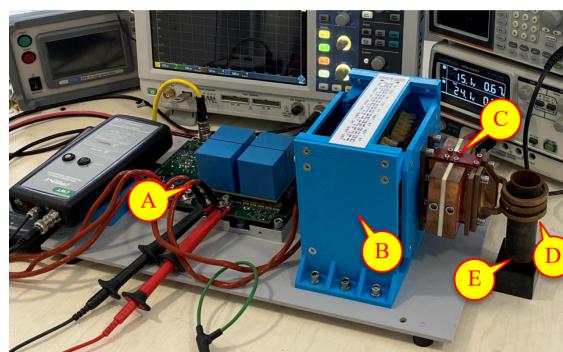


Figure 21. HB-SRI inverter test bed. Labels indicate items listed above.

Figures 22–24 show digital storage oscilloscope (DSO) measurements of the main waveforms of the HB-SRI inverter with PFM, EAPWM, and PDM control, respectively, for approximately 60% of the nominal output power. The expected output voltage, current, power, and frequency values were accurately obtained, despite the variability in the actual values of the components used.

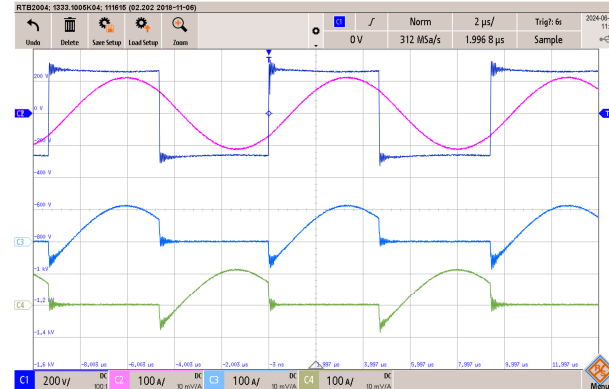


Figure 22. Experimental waveforms of the PFM HB-SRI inverter. C₁ (dark blue) is the output voltage (200 V/div), C₂ (magenta) is the output current (100 A/div), C₃ (light blue) is the current trough Q₁ (100 A/div), and C₄ (green) is the current trough Q₂ (100 A/div). Time base is 2 μs/div.

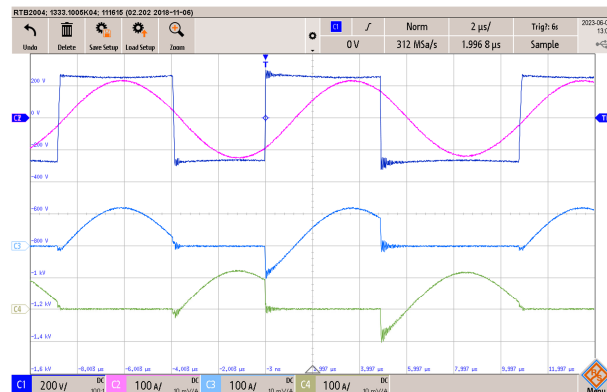


Figure 23. Experimental waveforms of the EAPWM HB-SRI inverter. C₁ (dark blue) is the output voltage (200 V/div), C₂ (magenta) is the output current (100 A/div), C₃ (light blue) is the current trough Q₁ (100 A/div), and C₄ (green) is the current trough Q₂ (100 A/div). Time base is 2 μs/div.

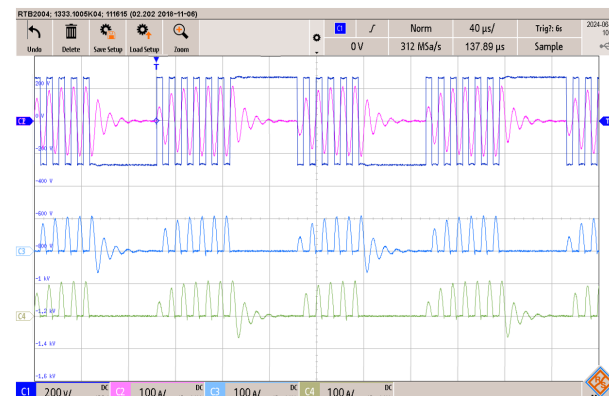


Figure 24. Experimental waveforms of the EPDM HB-SRI inverter. C₁ (dark blue) is the output voltage (200 V/div), C₂ (magenta) is the output current (100 A/div), C₃ (light blue) is the current trough Q₁ (100 A/div), and C₄ (green) is the current trough Q₂ (100 A/div). Time base is 40 μs/div.

Figure 25 shows the experimental efficiency measurements of the three modulations, all exceeding 98% for the maximum output power. The lines connecting the experimental points, marked with different symbols, are red for PFM, blue for EAPWM, and green for EPDM. Note that there were some differences between the experimental and calculated results, which may have been due to the modelling method used, the existence of losses of other elements not taken into account in the calculation (capacitors, conductors, parasitic components, voltage and current sensors, etc.), and also the measurement process.

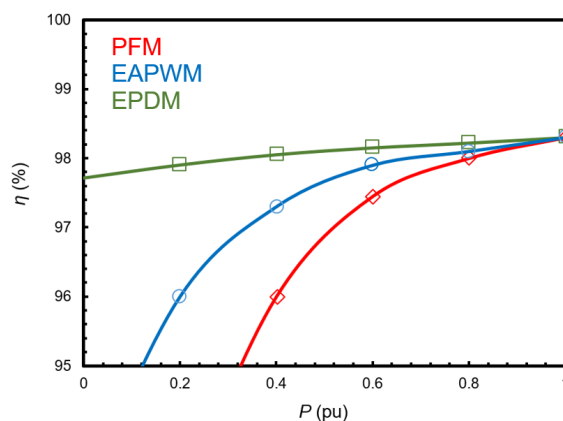


Figure 25. Experimental efficiency of HB-SRI inverter for different modulations as a function of normalized output power for PFM (red), EAPWM (blue) and EPDM (green).

4. Conclusions

The purpose of this work was to review the main characteristics of an HB-SRI inverter with SiC MOSFETs, operating with different modulations to regulate the output power. A complete design procedure and a comparative analysis of power losses and operating frequency variation have been presented. The results of the comparative study allowed determining that an HB-SRI inverter with EPDM is a cost-effective solution that incorporates the following improvements:

- The output power is regulated without varying the phase shift between the switches that compose the HB, and therefore, the efficiency remains high throughout the entire power range.
- The control circuit was designed to perform in ZVS condition.
- The variation in operating frequency is virtually negligible.
- The introduction of the alternative configuration of the active mode in the classic PDM modulation results in the DC component of the output voltage being zero and the losses in the two switches being balanced.

The viability of this design was verified with the construction and testing of an 18 kW, 100 kHz HB-SRI using SiC MOSFET transistors in a high-frequency induction heating application.

Finally, it should be noted that the EPDM modulation could present some drawbacks, especially when the converter has a light load and when the required output power is very small. If these conditions arise in an application, EAPWM modulation also represents an efficient and easy-to-implement solution. It is also important to highlight that, in the case of load changes, significant voltage or current surges could appear in the inverter components. In this case, the frequency tracking circuit described in Section 2.2, Section 2.4, and Section 2.6, in combination with the output power control circuit, would allow compensating for these surges. This study could be the subject of a future article.

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